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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

KONNO et al

Serial No.: 07/743,383 Group Art Unit: 1104

Filed: August 21, 1991 Examiner: G. Goudreau

For: METHOD FOR PRODUCING SEMICONDUCTOR INTEGRATED CIRCUITS AND APPARATUS USED IN SUCH METHOD

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

January 7, 1993

Sir:

In compliance with applicants duty of disclosure under 37 CFR 1.56, the following is material information of which applicants are aware and was cited in the attached European Search Report.

1. European Patent Appln. No. 0 416 774 dated 3/13/91
2. Solid State Technology, v. 33, no. 2 (Feb. 1990)
3. Extended Abstracts, vol. 81-2 (1981) pp. 715-716
4. Japanese Patent Abstract of JP-A-1 251 742 (Jan. 1989)
5. European Patent Appln. No. 0 345 757 dated 12/13/89
6. European Patent Appln. No. 0 387 097 dated 9/12/90

Commissioner is hereby authorized to charge the necessary fee of $200.00 to Deposit Account No. 14-1060. A duplicate of this sheet is attached herewith.

In the event that any additional fees are due with this paper, please charge Counsel's Deposit Account No. 14-1060.

Respectfully submitted,

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Atty. Case No. P698-1333

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Enclosures: Information Disclosure Citation, European Search Report and References (6)